In the Specification:

Please amend paragraph 0001 on page 1 as follows:

The present invention relates to methods of interconnecting layers of semiconductors on a wafer substrate by tungsten plugs and more particularly a method of producing tungsten plugs or vias filled with tungsten for connecting semiconductor layers having reduced pullout characteristics during the chemical milling processing of a 300 ~~μm~~ mm wafer.

Please amend paragraph 0002 on page 1 as follows:

As is well known by those skilled in the art, increasing yield is one of the primary goals of any change in the fabrication of semiconductors devices. For example only, if a 200 ~~μm~~ mm silicon wafer has space for 100 IC's or integrated circuits, the amount of yield would be 100 percent if all 100 IC's passed all of the functional and operational tests. Although a 100 percent pass rate would be unusual, there are other ways to reduce costs. For example, if a 200 ~~μm~~ mm wafer having an area of 31,400 square ~~μm~~ mm = ($\pi d^2/4$) then a 300 ~~μm~~ mm wafer having 70,650 square ~~μm~~ mm should produce over 200 similar IC's. In other words, over twice the number of IC's. Since the process times and steps for a 200 ~~μm~~ mm wafer and a 300 ~~μm~~ mm wafer would be substantially the same, it is obvious that if the cost of a 300 ~~μm~~ mm wafer is proportional to the area increase over a 200 ~~μm~~ mm wafer, then increasing the wafer size should reduce manufacturing costs. Consequently, 300 ~~μm~~ mm wafers are available at competitive prices and many, if not most, manufacturing processes are switching over to 300 ~~μm~~ mm wafers.

Please amend paragraph 0003 on pages 1 and 2 as follows:

Unfortunately, as always seems to be the case, an improvement in manufacturing techniques in one area either amplifies minor existing yield problems or introduces completely new yield problems. One yield problem that has become significant with 300 ~~μm~~ mm wafers is the "pullout" during CMP (chemical mill processing) of tungsten (W) plugs used to connect circuit levels in a multilevel IC.

Please amend paragraph 0004 on page 2 as follows:

The problem was almost non-existent with the prior art 200 ~~μm~~ mm wafers, but is not at all unusual while processing 300 ~~μm~~ mm wafers. The problem is believed to result because of differences in thermal expansion of materials deposited on the silicon wafer. It is well-known that films deposited over silicon always cause some sort of stress. As examples, depositing an oxide film typically causes compressive stress whereas depositing a metal film over silicon typically causes tensile stress. The resulting stress usually manifests itself as wafer warpage, and increasing the wafer size from 200 ~~μm~~ mm to 300 ~~μm~~ mm has increased the wafer warpage significantly enough to cause the tungsten plug to pullout or pull-up at the center of the larger wafer.

Please amend paragraph 0010 on page 5 as follows:

FIG. 2 illustrates a typical tungsten plug pullout on a 300 ~~μm~~ mm wafer;

Please amend paragraph 0015 on page 6 as follows:

Referring now to FIG. 1, there is illustrated a typical layout of about 122 integrated circuits, such as 10a, 10b, 10c and 10d, on a silicon wafer 12. As was discussed above, adding oxide and/or metal films on top of silicon wafer always causes some stress in the structure (oxide films typically cause compressive stress and metal films typically cause tensile stress). As was also discussed, processing steps such as CMP (chemical milling processing) or fabricating tungsten (W) plugs as interconnecting lines between multiple layers of circuits in an IC (integrated circuit) results in an unacceptable number of tungsten plug "pullouts" or "pull-ups" in the chips processed on a 300 ~~μm~~ mm wafer whereas such "pull-outs" are not a major concern when the CMP is with respect to a smaller 200 ~~μm~~ mm wafer.